IN THE SPECIFICATION

Please replace the following paragraphs in the Specification with the rewritten paragraphs below:

[0011] FIG. 4 is another block diagram illustrating an amplitude ~~control~~ calibration unit coupled to a voltage controlled oscillator.

[0040] Co-pending and commonly assigned U.S. patent application serial number 10/092,669, entitled CALIBRATION TECHNIQUES FOR FREQUENCY SYNTHESIZERS, filed on March 6, 2002 for Jeremy D. Dunworth *et. al*, ~~and bearing attorney docket number 010481,~~ describes frequency calibration techniques for a frequency synthesizer and is hereby incorporated herein by reference in its entirety. In embodiments described in the above-identified application, the PLL of an oscillator may be disabled for frequency calibration. Accordingly, the amplitude calibration techniques described herein may be performed in parallel with frequency calibration techniques, such as those described in the above-identified application in order to avoid any additional down-time to PLL 31 during amplitude calibration. Also, by performing amplitude calibration techniques in parallel with frequency calibration techniques, the amplitude calibration routine may be modified to account for any adjustments to resistance in the oscillator tank of the VCO (which may affect amplitude), such as changes in resistance that result from the activation or deactivation of capacitor switches.

[0042] FIG. 6 is a block diagram of a frequency synthesizer 20 implementing discrete frequency calibration of VCO 30 and discrete amplitude calibration of VCO 30 in parallel. In this example, VCO 30 includes a configurable tail current source as outlined above. In addition, VCO 30 may include additional configurable circuitry so that frequency calibration can be performed at the same time as amplitude calibration. For example, VCO 30 may include a number of switched capacitors that facilitate adjustments to the capacitance of the oscillator tank of VCO 30. In general, one or more of a variety of different frequency calibration techniques may be implemented when PLL is disabled. In the example of FIG. 6, however, the frequency calibration technique used is one described in the U.S. patent application serial number 10/092,669 mentioned above.